

Microelectronics: The Beginning of the End or the End of the Beginning?

- Texas GSP 1.5T\$ (top 12 in world)
- Economy transition from resource to tech-based post WWII
- Information technology
- Green energy

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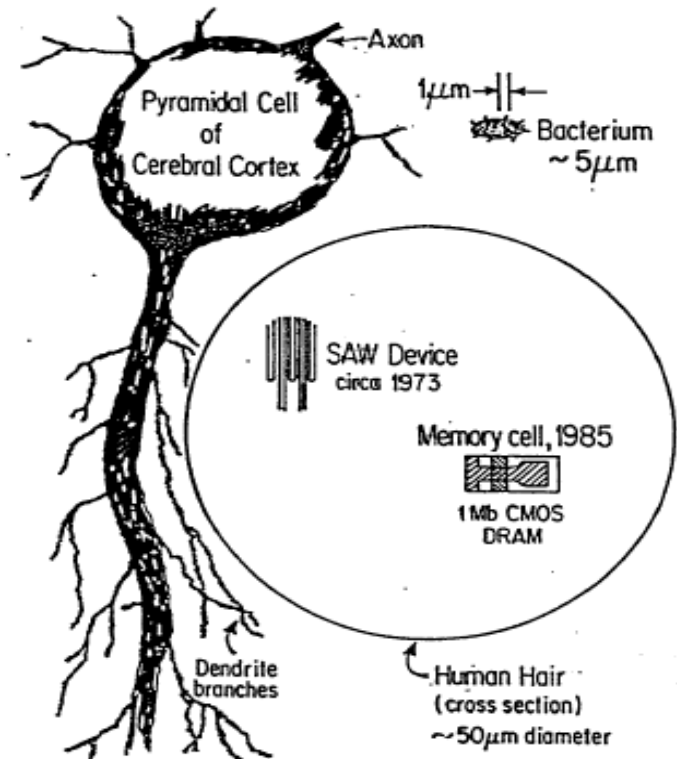
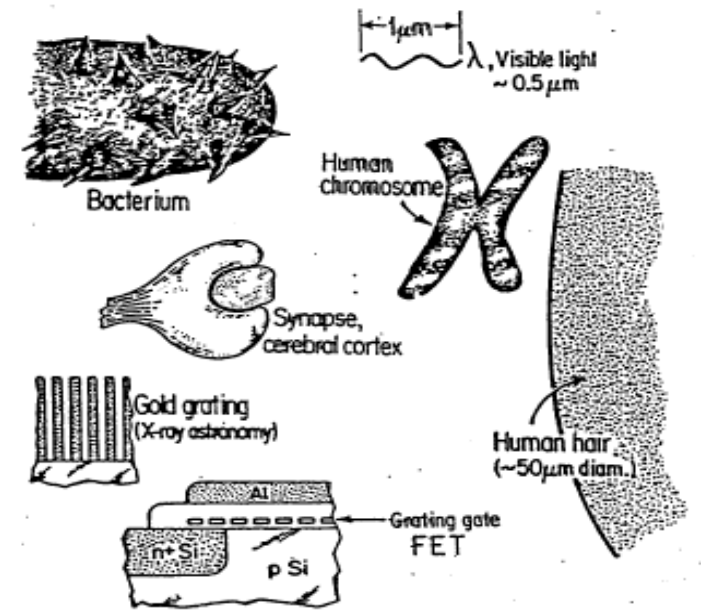
Moore's Law



No exponential is forever!

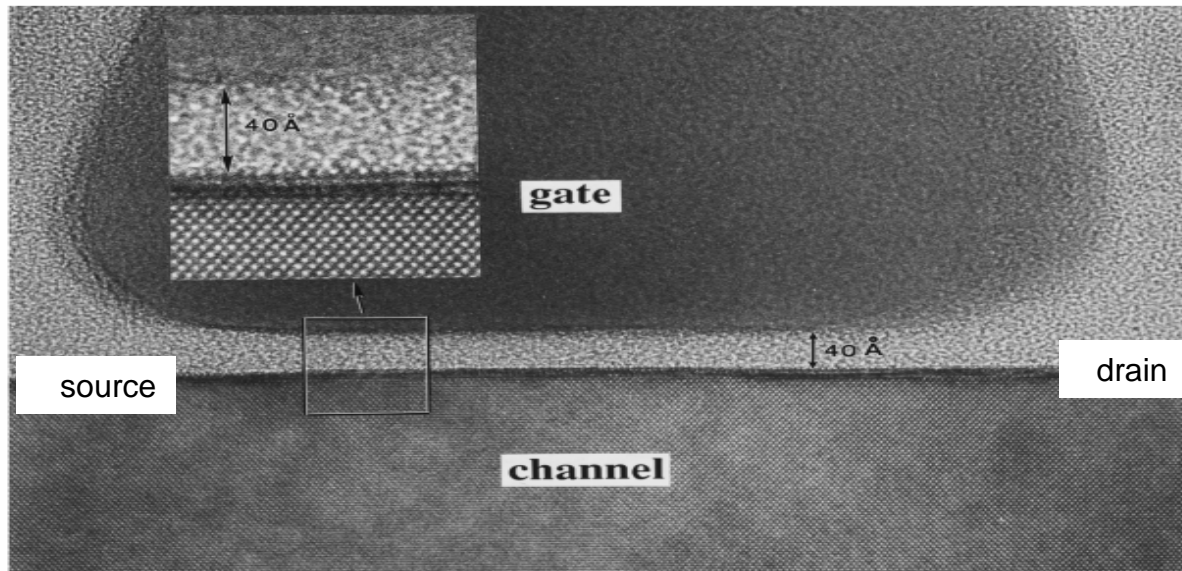
But can we delay "forever"?

Invention of the IC by Nobel Laureate Jack Kilby of TI in 1958

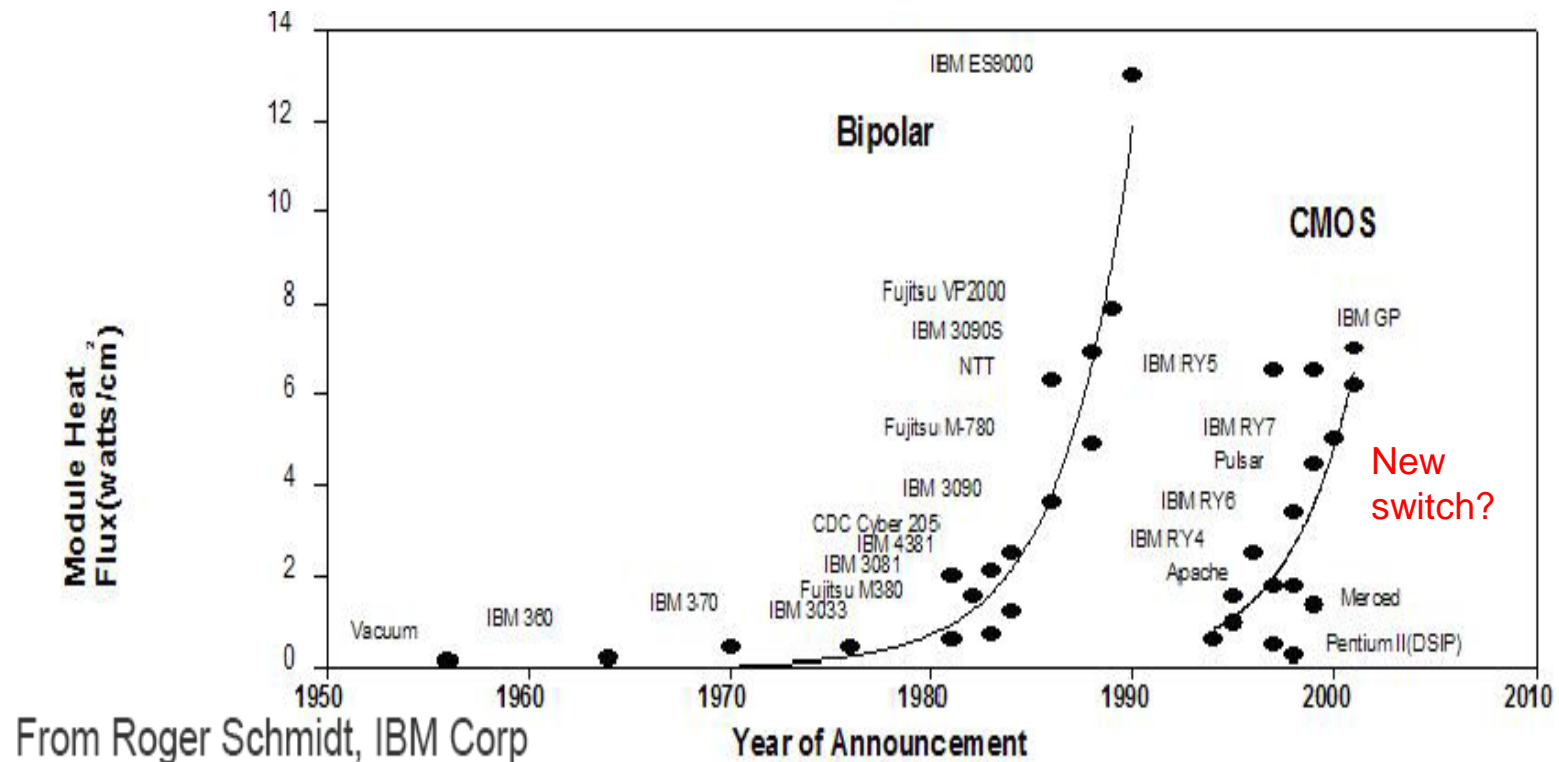


Societal Impact

- The \$300 billion IC industry drives a \$1 trillion electronics business, and has been the lifeblood of the Information Age for the past 50 years.
- Average person owns over a 100 billion transistors.
- 100,000 transistors would fit across, and cost less than a single grain of rice.



The Other Energy Crisis!



Opportunities for Transformation

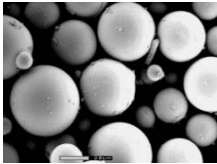
Things Natural



Dust mite
200 μm



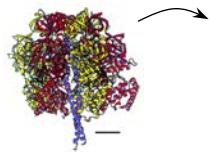
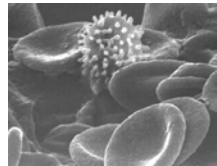
Ant
~ 5 mm



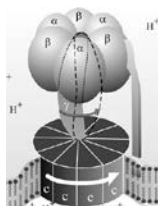
Fly ash
~ 10-20 μm

Human hair
~ 60-120 μm wide

Red blood cells
with white cell
~ 2-5 μm



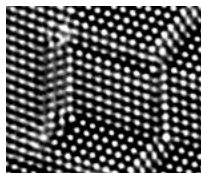
~10 nm
diameter



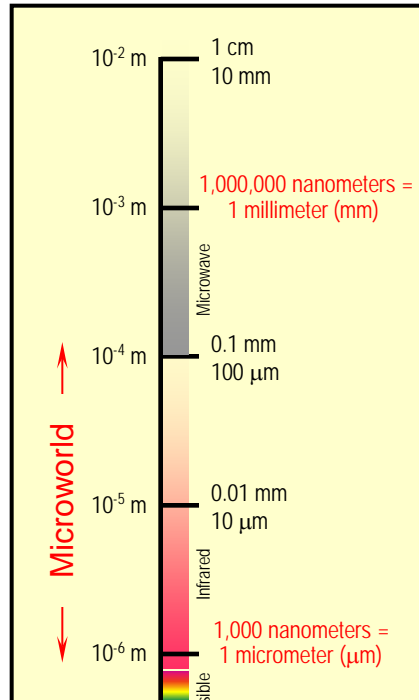
ATP
synthase



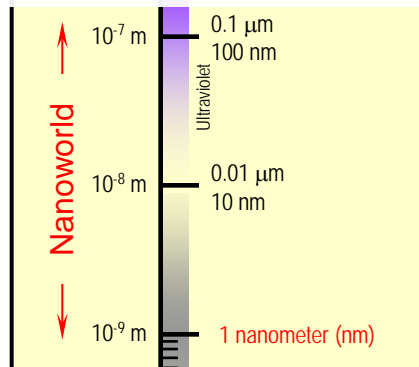
DNA ~2-1/2 nm diameter



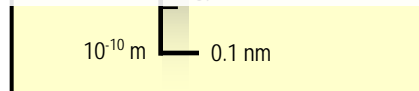
Atoms of silicon
spacing ~tenths
of nm



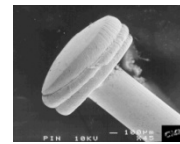
Smaller is different!



More is different!



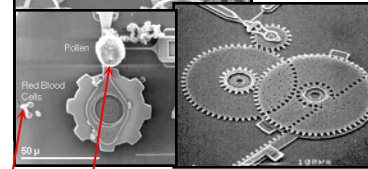
Things Manmade



Head of a pin
1-2 mm

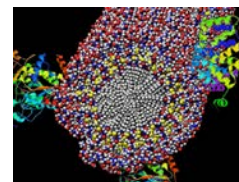


MicroElectroMechanica
I (MEMS) devices
10 -100 μm wide

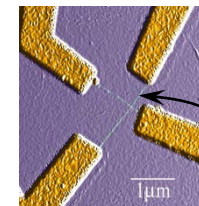


Pollen grain
Red blood cells

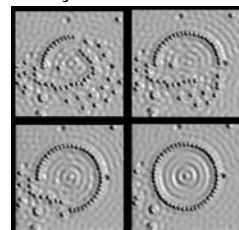
Zone plate x-ray "lens"
Outer ring spacing ~35 nm



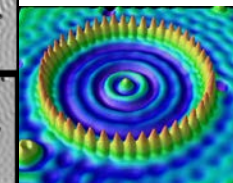
Self-assembled,
Nature-inspired structure
Many 10s of nm



Nanotube electrode

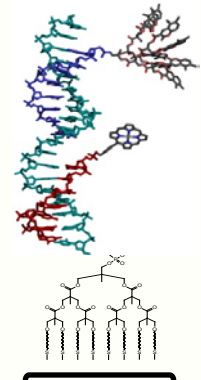


Quantum corral of 48 iron atoms on copper surface
positioned one at a time with an STM tip
Corral diameter 14 nm

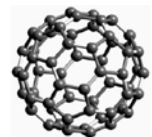


Carbon nanotube
~1.3 nm diameter

The Challenge



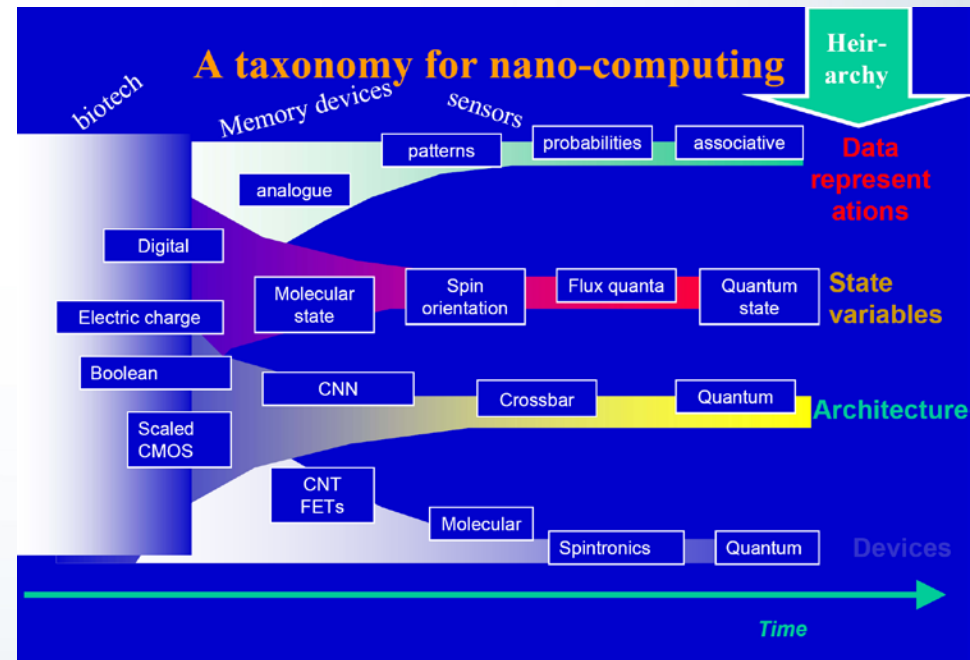
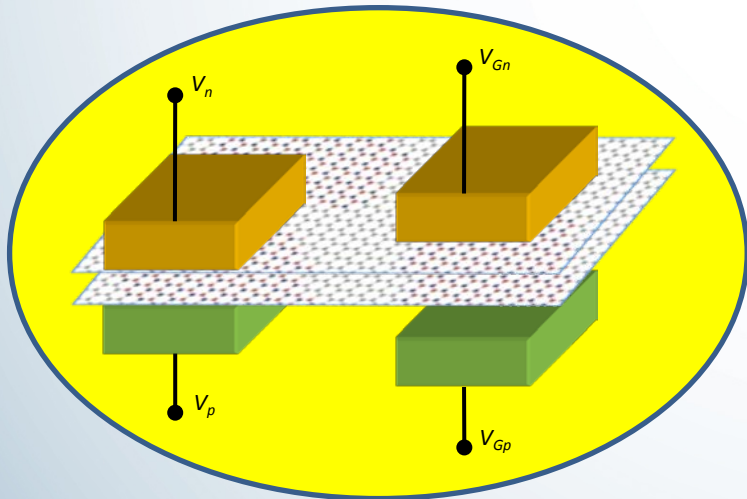
Fabricate and combine nanoscale building blocks to make useful devices, e.g., a photosynthetic reaction center with integral semiconductor storage.

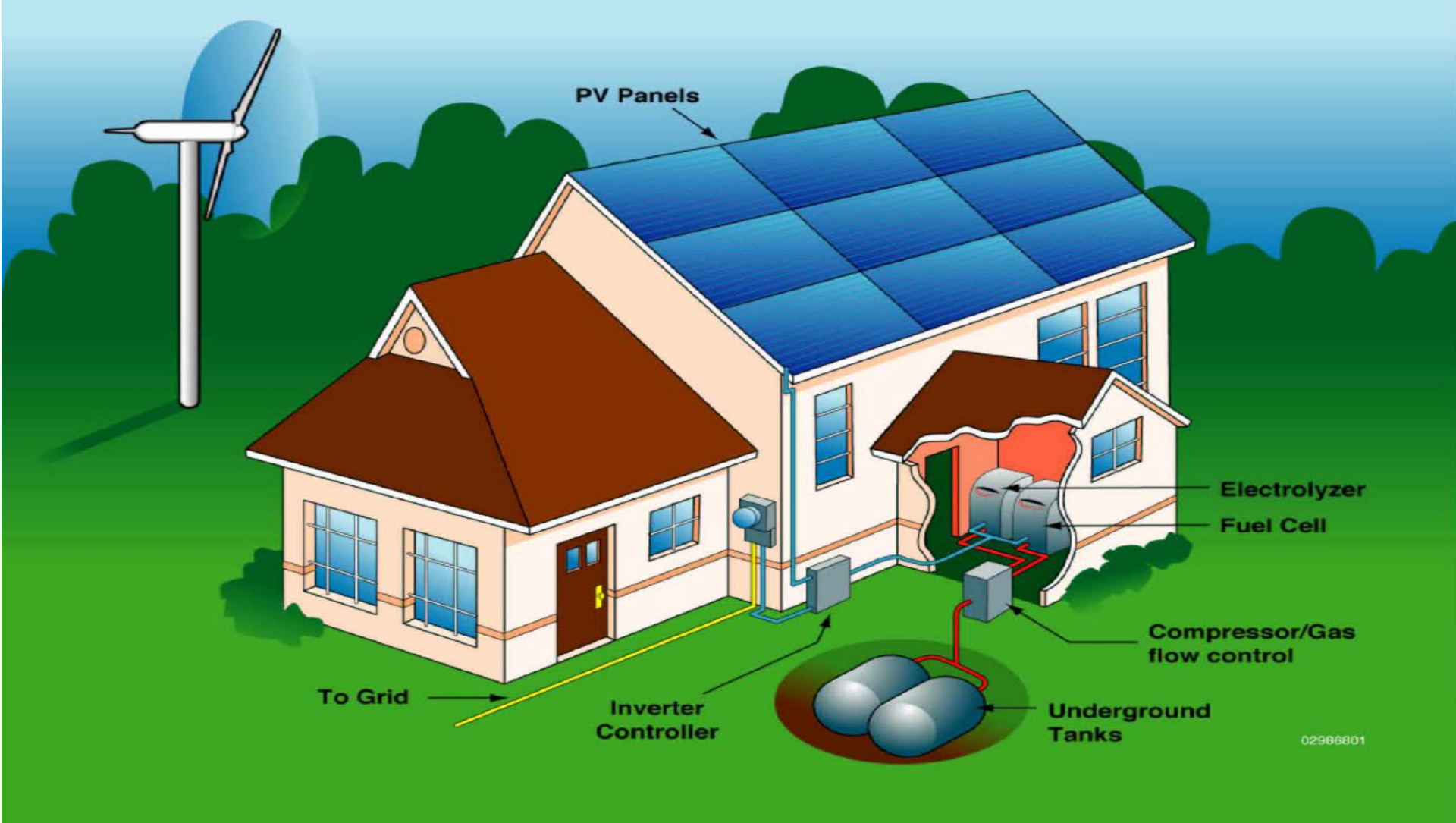


Carbon
buckyball
~1 nm
diameter

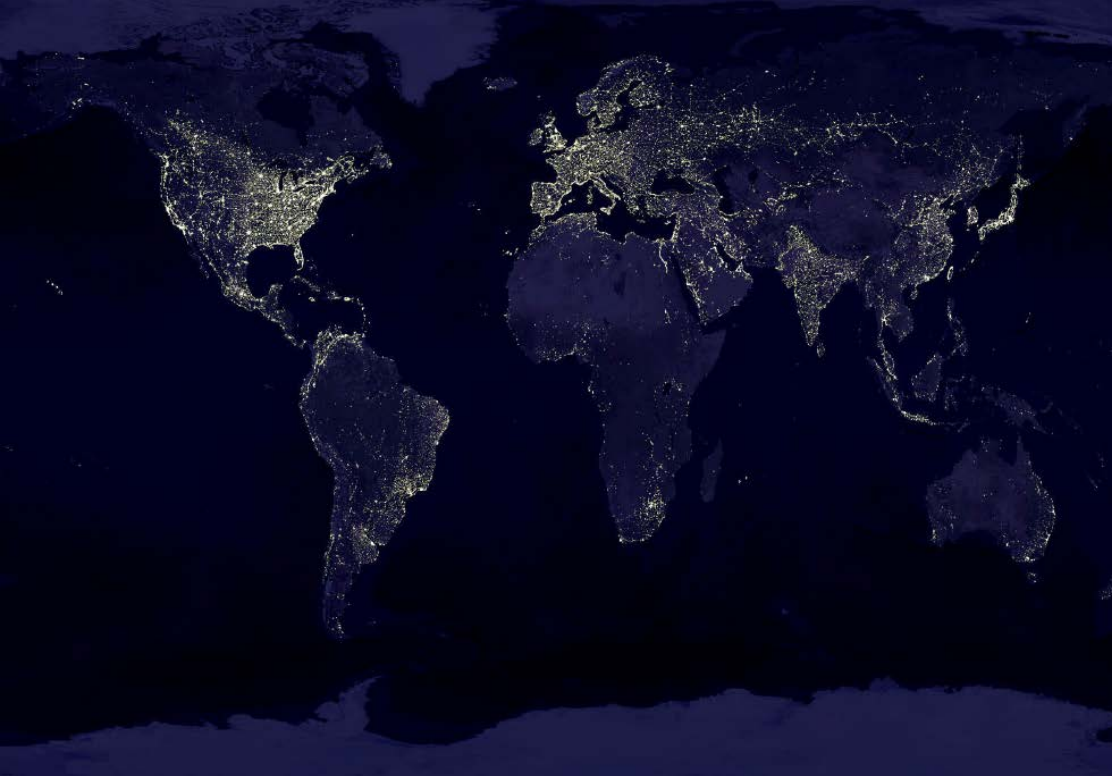
Strategic Paths to Innovation

- R&D investments in Tier 1 schools must increase to make us competitive with high tech powerhouses EU, Japan, ... and increasingly China.
- Example of successful partnership between Emerging Technology Fund of Texas, Texas Universities and Industry is the NRI South West Academy of Nanoelectronics at UT Austin, Dallas, Arlington, A&M & Rice: funded by Intel, IBM, TI, Micron, Global Foundries and NIST.
- The Bilayer Pseudospin Field Effect Transistor could consume 0.1% of the energy of conventional transistors if it can be made.





- Global energy demand is **15 TW** (US ~3 TW), $5E20J$; **50 TW** by 2100
- Currently ~1 % of generation is solar and wind; rest from fossil fuels, hydro and nuclear. There is $5E24J$ of non-renewable fossil and nuclear fuel available.

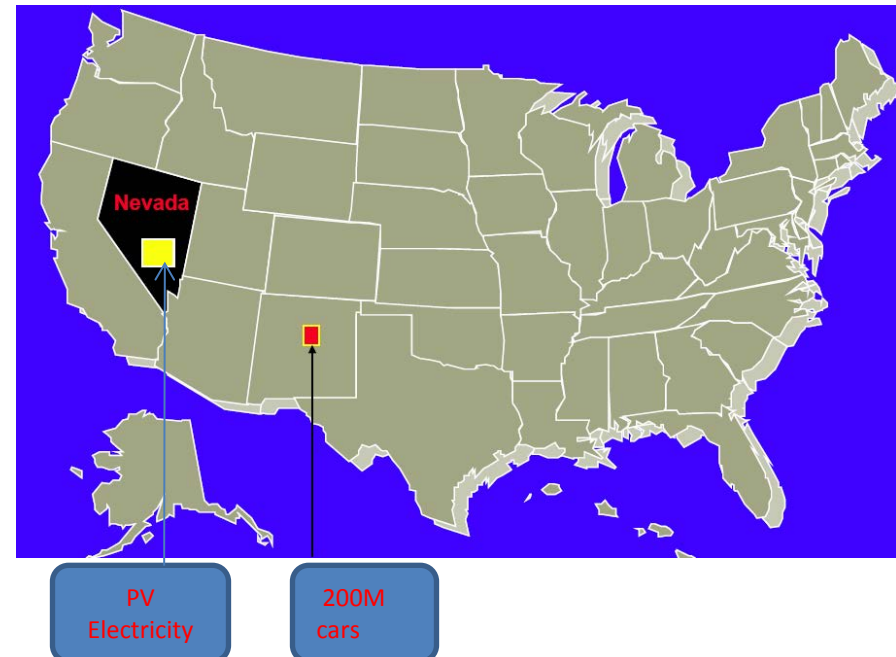
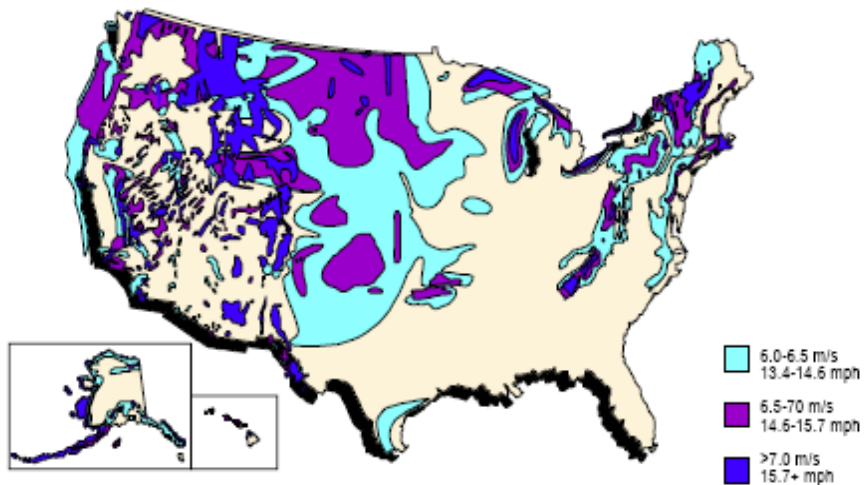


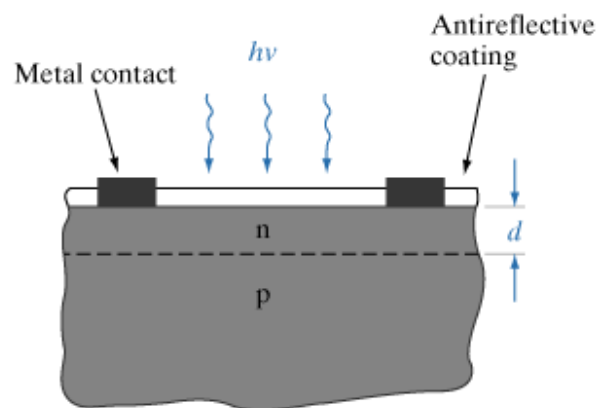
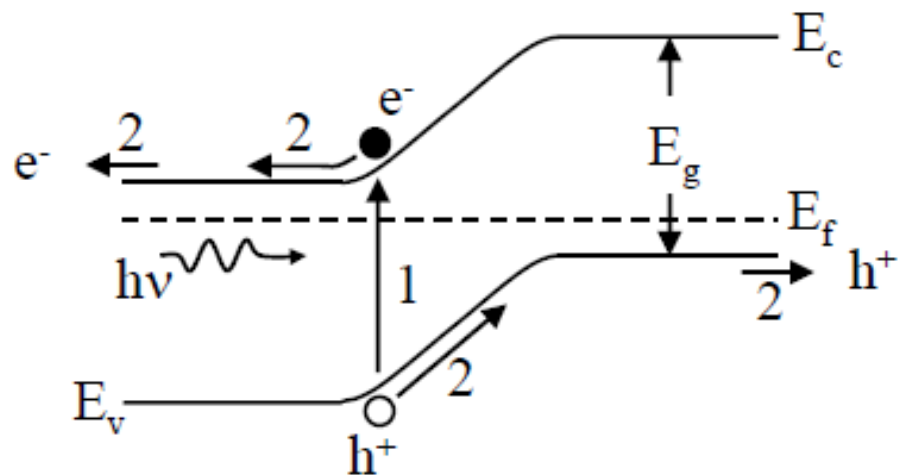
- There is 100,000 TW of solar power and 1700 TW of wind power; of this 6000 TW of solar and 100 TW of wind power are accessible. Total power is **8000** times current need.

- Solar and wind generation sites often far from cities- hence **smart power grid** critical

- Solar and wind suffer from intermittency problems- hence **storage** is critical

Wind





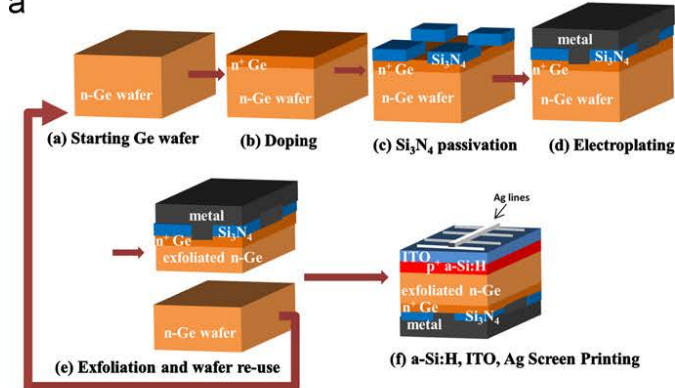
(a)



(b)

Figure 8-5

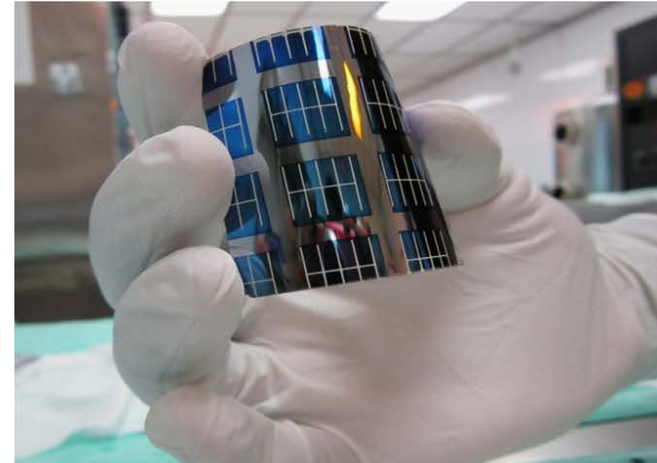
Configuration of a solar cell: (a) enlarged view of the planar junction; (b) top view, showing metal contact "fingers."

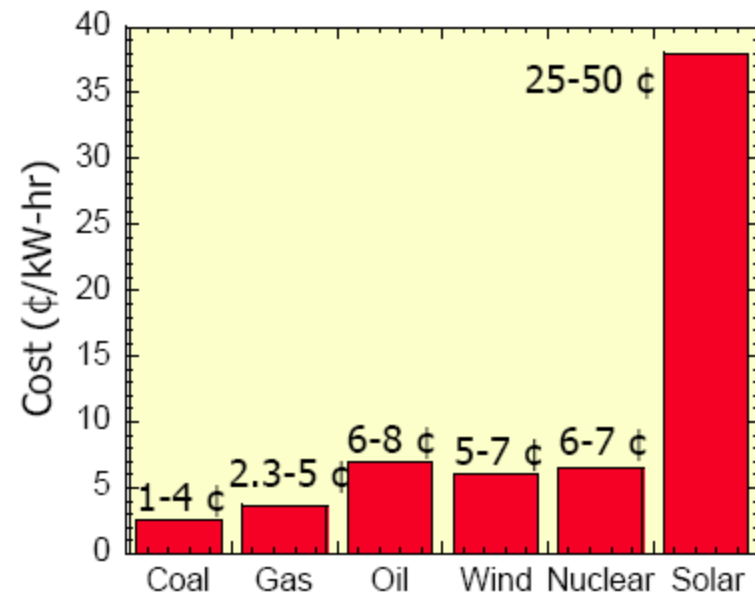
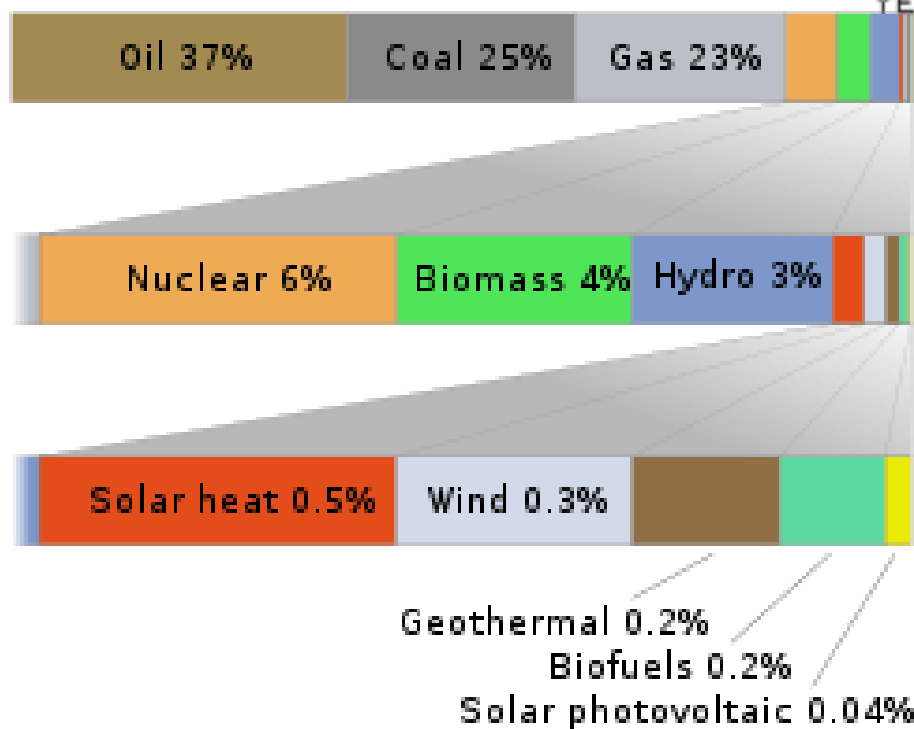
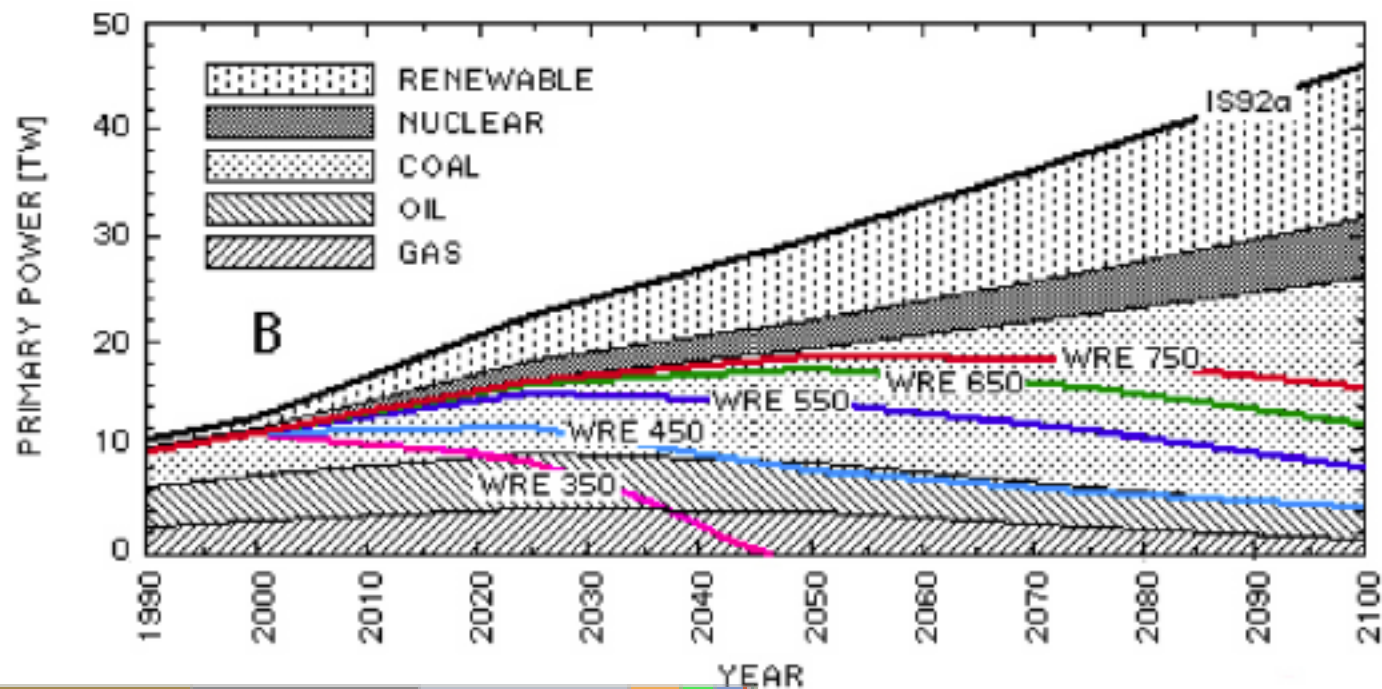


b

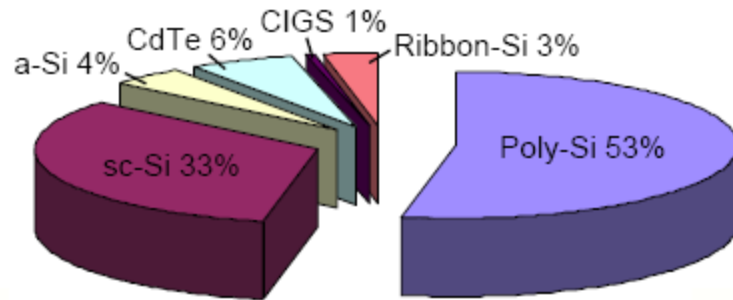


c





Industry Breakdown 2007



Requirements

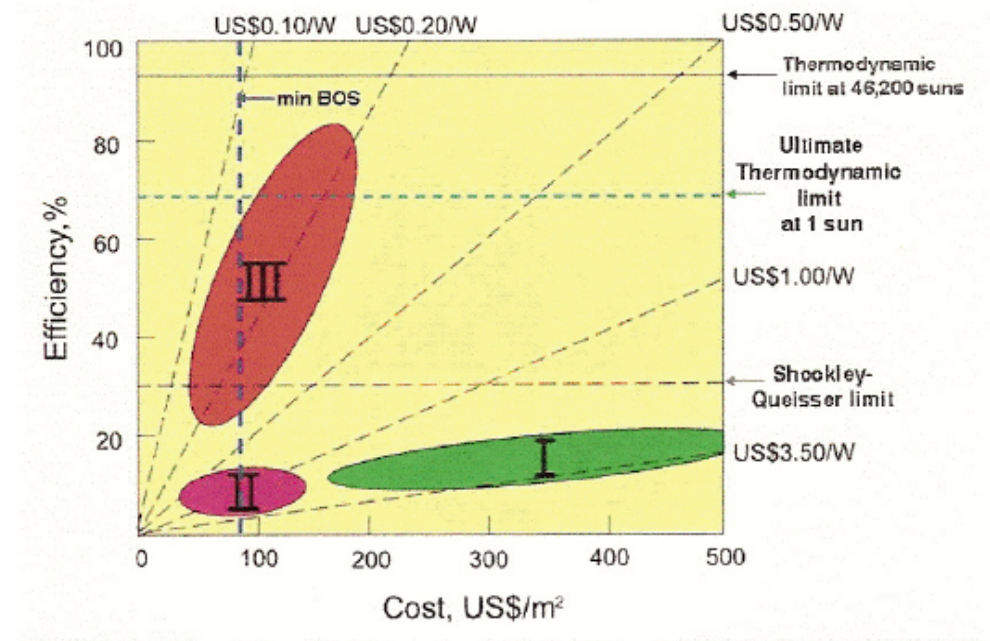
- Efficiency $\sim 50\%$
- Cost $\sim \$0.20/W_p$

Currently

- Efficiency $\sim 15\%$
- Cost $\sim \$3.50/W_p$

Improvement

- Cost $\sim 15\times$
- Efficiency $\sim 3\times$
- FoM: Efficiency/Cost Ratio ($\%W/\$$)



3rd Generation Solar Cells

As function of module efficiency and areal cost

Epilog: the 10 gallon economy in 2050

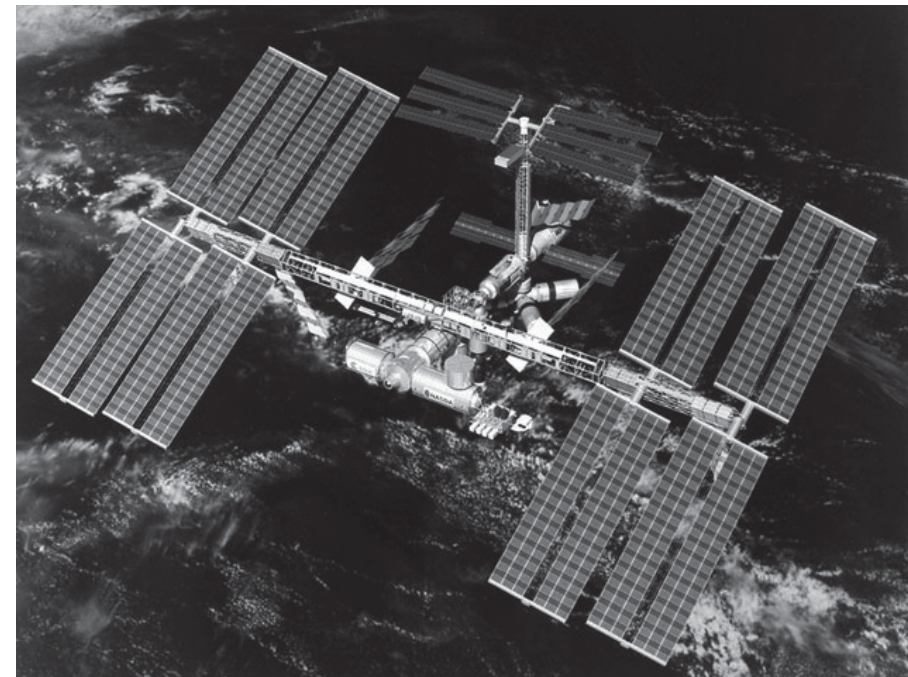
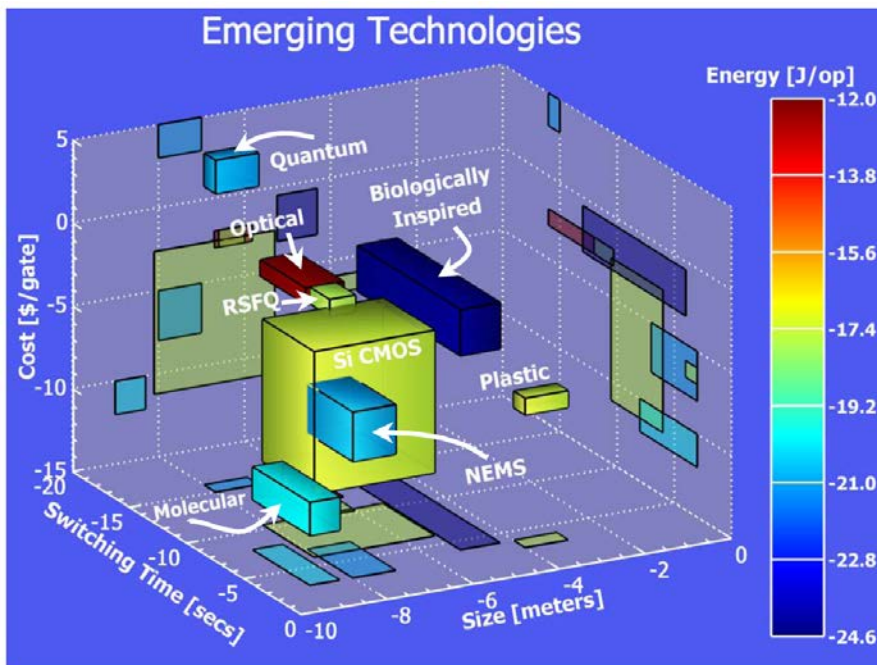
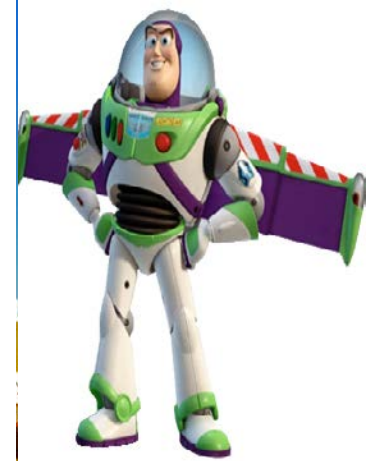
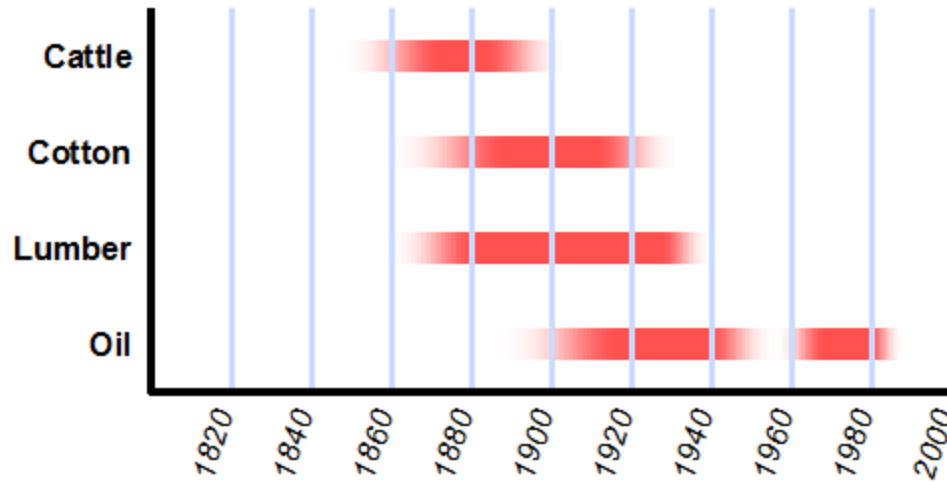


Figure 42 Parameterization of Emerging Technologies and CMOS—Speed, Size, Cost, and Switching Energy